

PROTEUS

The Complete Electronics Design System

VSM

Virtual System Modelling

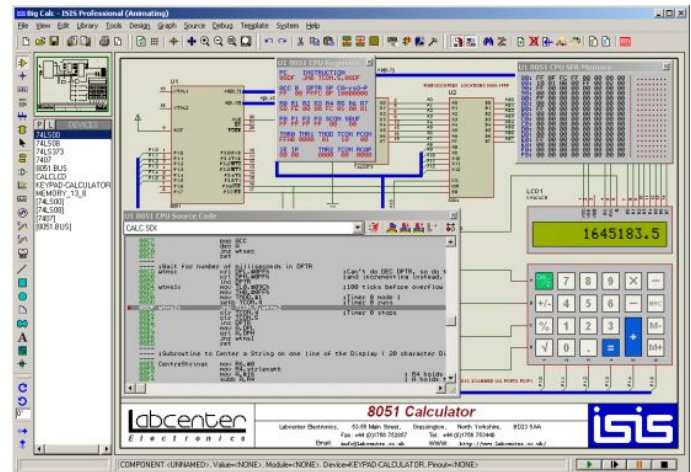
System Features

- ISIS Schematic Capture - an easy to use yet extremely powerful tool for entering your designs.
- PROSPICE Mixed mode SPICE simulation - industry standard SPICE3F5 simulator upgradeable to our unique Virtual System Modelling technology.
- ARES PCB Layout - ultra high performance PCB design system with 32 bit database, automatic component placer and rip-up and retry auto-router.
- Modern Graphical User Interface standardized across all modules.
- All major modules written in house - best possible guarantee of inter-operability and compatibility.
- Runs on Windows 98/Me/2K/XP or later.
- Established, proven product based on more than 15 years of continuous development.
- Thousands of installations sold to over 35 countries worldwide.
- Technical support direct from the authors.
- Rated best overall product in EWW CAD Review Roundup.

PROTEUS combines advanced schematic capture, mixed mode SPICE simulation, PCB layout and auto-routing to make a complete electronics design system.

The system benefits from over 15 years of continuous development, and was rated the best all round product by Electronics World in its comparative review of PCB design systems - "The Route to PCB CAD".

The PROTEUS product range also includes our revolutionary VSM technology, which allows you to simulate micro-controller based designs, complete with all the surrounding electronics. You can even interact with your design in real time using animated peripheral models for LED/LCD displays, keypads, RS232 terminals and so forth.



Meanwhile our acclaimed auto-placer and auto-routing tools continue to make PCB layout as easy as possible, with the hard work being done by your PC rather than yourself.

As a Professional user, you will have unlimited access to our dedicated technical support line, whilst we also provide at least four upgrades a year through our upgrade subscription service.

Our overriding philosophy remains that of continuous product development - an approach that keeps PROTEUS one step ahead of the competition.

labcenter
Electronics

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Intelligent Schematic Input System

ISIS lies right at the heart of the PROTEUS system and is far more than just another schematics package. It combines an exceptionally powerful design environment with the ability to control most aspects of the drawing appearance. Whether your requirement is the rapid entry of complex designs for simulation & PCB layout, or the creation of attractive schematics for publication, ISIS is the tool for the job.

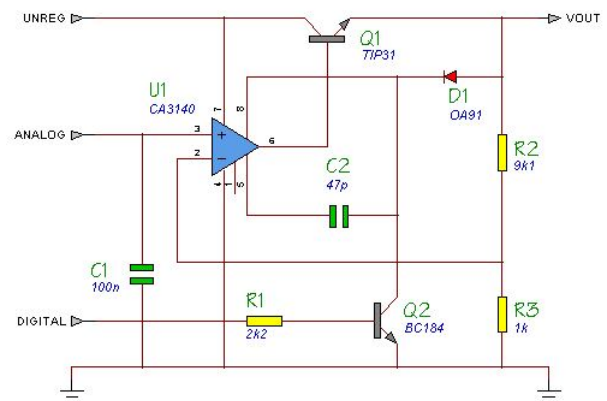
Schematic Capture

Features

- Produces publication quality schematics.
- Style templates allow customization of supplied library parts.
- Mouse driven, context sensitive user interface.
- Automatic wire routing and junction dot placement/removal.
- Hierarchical design including parameterization of sub-circuit component values.
- Full support for buses including sub-circuit ports and bus pins.
- Preview of PCB footprints whilst selecting components and making new library parts.
- Comprehensive representation for homogenous and heterogeneous multi-element parts including connectors.
- Sophisticated management of component properties including customization of the relevant dialogue forms.
- Large and growing component library of over 8000 parts, most complete with ready to use simulator models.
- Netlist formats: Labcenter SDF, SPICE, SPICE-AGE, Tango, Boardmaker, EEDesigner, Futurenet, Racal & Valid.
- Electrical Rules Check and Bill of Materials reports.
- Output to any Windows printer device in colour or monochrome.
- Graphical export in WMF, BMP, DXF, EPS and HPGL formats.

Publication Quality Schematics

ISIS provides you with full control of the drawing appearance in terms of line widths, fill styles, colours and fonts. This enables you to produce attractive schematics like you see in the magazines rather than the 'thin line' diagrams often associated with older CAD software. Once your drawing is complete you can export it as a graphics file or copy it to the clipboard for incorporation in other documents. This makes ISIS ideal for use in producing technical documentation, academic papers, project reports, as well as being an excellent front end for PCB design.



The drawing appearance is defined in terms of a style template - especially useful if you want to apply a 'house style' to all your designs. Furthermore, the scheme allows you to customize the appearance of the library parts supplied with the package.

Context Sensitive User Interface

Much thought has gone into making the most common drawing operations as quick and easy as possible. In particular, ISIS has no wiring mode per se. Instead, you can place a wire at any time by clicking on a component pin or on a previously placed wire. In addition, place, edit, move and delete operations can be achieved directly with the mouse, without having to go through menus or icons. This makes ISIS very quick to use indeed.

Wire Auto-Router

Placing a wire can be as simple as clicking on the two pins you want to connect - the Wire Auto-Router does the rest. But if you want a wire in a particular place, you can just click at the intermediate corners. The Wire Auto-Router also operates when components are moved, automatically fixing up the affecting wiring.

Junction dots are placed and removed automatically. As well as saving time, this avoids ambiguities that might otherwise arise. Manual placement of dots is also allowed, should you prefer to place a dot and then wire to it.

Hierarchical Design

As well as supporting normal multi-sheet designs (equivalent to a circuit spread over several pieces of paper), ISIS supports hierarchy within a design. In other words, a particular component can be defined as a module which is then represented by a further circuit diagram. The hierarchy can be nested to an arbitrary number of levels, and modules can be drawn as standard components, or as special sub-circuit blocks on which the interface ports can be placed and removed on the fly.

Full Support for Buses

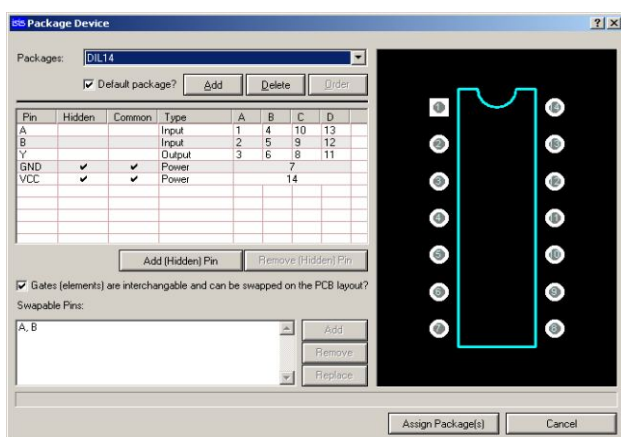
Buses are used to represent multiple parallel connections, typically for data or address lines in microprocessor designs. ISIS provides not only a bus wire, but also the ability to define components and sub-circuits with bus pins. Therefore, a 32 bit processor bus connection between processor and memory can be represented as a single wire, saving both drawing time and space on the diagram.

Device Libraries

ISIS comes with a device library including over 8000 parts. The libraries include standard symbols, transistors, diodes, thermionic valves, TTL, CMOS, ECL, microprocessor and memory parts, PLDs, analog ICs and op-amps as well as manufacturer specific libraries from National Semiconductor, Philips, Motorola, Teccor, Texas and Zetex. More libraries are being created as part of an ongoing programme.

Visual Packaging Tool

Matching schematic and pcb library parts is greatly simplified by the packaging tool. This displays the PCB footprint alongside the pins of the schematic part and allows both textual and graphical entry of pin numbers for each pin name.



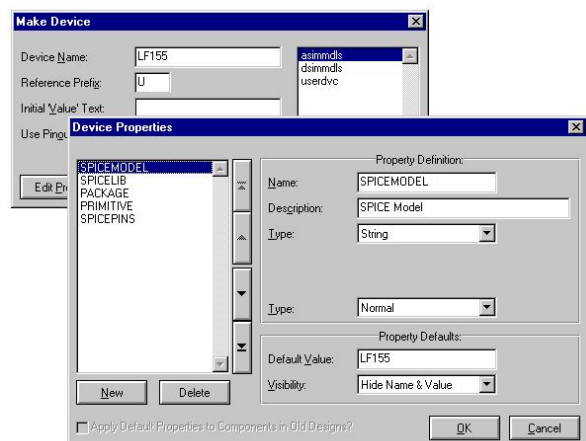
Multi-Element Parts

The way in which ISIS represents library parts allows for all the common possibilities: single element (e.g. 555 timer), homogenous multi-element (four 7400 gates), and heterogenous multi-element (relay coil and contacts). Connectors can also be represented as individual pins such that they can be distributed across the schematic, rather than having to wire everything back to a single part.

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Component Properties

Each component in your design can have an arbitrary number of properties or attributes. Some properties control specific functions of the software (e.g. PCB package, or simulator model) but you can also add your own properties to hold other information such as stock codes or component costs. Furthermore, when a library part is created, default values and 'Property Definitions' can be supplied. Property definitions provide a plain English description of the property and cause it to be displayed in its own editing field when the component is edited. You can even specify appropriate range limits for numeric values, and keyword lists for strings. A special type for PCB packages allows for browsing of the ARES libraries.



Report Generation

ISIS supports many 3rd party netlist formats making it suitable as a front end for use with other software.

The Bill of Materials report can be configured to include whichever component properties you wish, and can also include column totals for selected numeric properties.

Equally useful is the ERC report which lists possible wiring mistakes such as unconnected inputs, conflicting outputs and mis-typed net-labels.

“The revamped schematic drawing section is quick, versatile, and gives good graphics quality - recommended if your schematics are to be plotted out for professional use.”

“The choice of manually drawing the connections or using the excellent wiring autorouter remains. Both are well-designed systems, easy to use and effective.”

Electronics & Wireless World Review

PROSPICE is a state of the art mixed mode circuit simulator that operates in conjunction with the ISIS schematic capture environment. Based around the industry standard SPICE3F5 analogue kernel, with our own extensions for mixed mode simulation and interactive circuit animation, PROSPICE provides a powerful, interactive environment in which to develop and test your designs.

System Features

- Fully integrated with schematic capture environment.
- Supports both Graph Based and Interactive Circuit Simulation with virtual instruments and user definable animated components.
- Unique Proteus VSM technology allows co-simulation of Microprocessor Designs.

Analogue Simulation

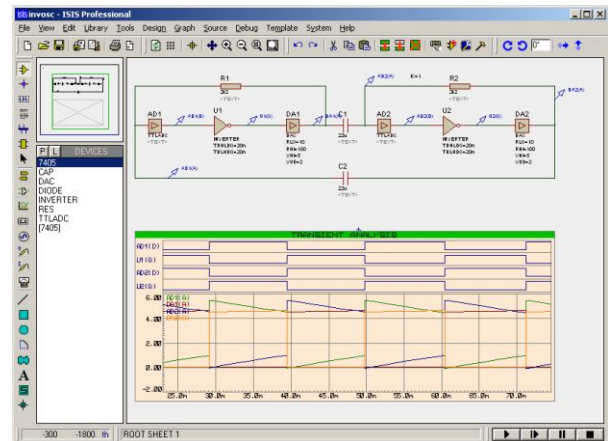
- Genuine Berkeley SPICE3F5 analogue simulator kernel with extensions for true mixed mode operation.
- Graph Based Analyses: Operating Point, Transient, Frequency, DC Transfer Curve, DC Parameter Sweep, AC Parameter Sweep, Noise, Distortion, and Fourier, Input & Output Impedance.
- Advanced primitives include MOSFET Level 3, BSIM version 3, MESFET, lossy transmission line and expression based arbitrary source.
- Direct compatibility with manufacturers' SPICE models.
- Over 6000 models supplied with the package.

Digital Simulation

- Event driven digital simulation models timing, glitch and floating input behaviour.
- Fusemap models allow simulation of PLDs directly from JEDEC files.
- Full set TTL and CMOS models complete with timing information.
- Conformance analysis facilitates automatic testing of embedded systems.

Fully Integrated Environment

Circuit simulation within PROTEUS is conducted entirely from within the ISIS schematic capture module. Graphs appear alongside the components on the schematic, with circuit stimuli (generators) and probes being placed directly on the wiring. The circuit can be simulated at any time by pressing the space bar, making the edit-simulate cycle extremely rapid - far more so than in packages where the simulator has its own application window and user interface.



Graph Based or Interactive Simulation

In addition to traditional graph based circuit simulation, PROSPICE offers fully interactive circuit animation. You can control your design using mouse operated component models (e.g. switches, pots) and observe what is happening from on screen indicators (e.g. LEDs, 7 seg. displays, meters). Uniquely, it is possible to design your own actuators and indicators, making the system suitable for modelling the actual peripherals of a real design.

Additionally, numerous virtual instruments are provided including Voltmeters, Ammeters, an Oscilloscope, a Logic Analyser a Signal Generator, and Digital Pattern Generator. These operate in much the same way as their real world counterparts, making for a very intuitive approach to circuit simulation.

Upgradable to Proteus VSM Co-Simulation

Should your designs include microprocessors such as the PIC, AVR, MCS8051/52, or 68HC11, you purchase additional VSM models for these parts. This unique technology allows you to simulate complete microcontroller based designs, including all the associated electronics at speeds approaching real time. Please refer to the separate Proteus VSM brochure for more information.

Partial Simulation of Large Designs

Where PROTEUS is being used to enter an entire design for PCB layout, it may be inappropriate to run simulation experiments on the entire schematic. For example, it doesn't usually make sense to simulate crystal oscillators as analogue circuits when testing the digital logic that they drive. PROSPICE saves you from carving up the schematic by supporting partial simulation of the design. The circuit topology is analysed and only those components located between the input stimuli and the measurement points are included in the simulation.

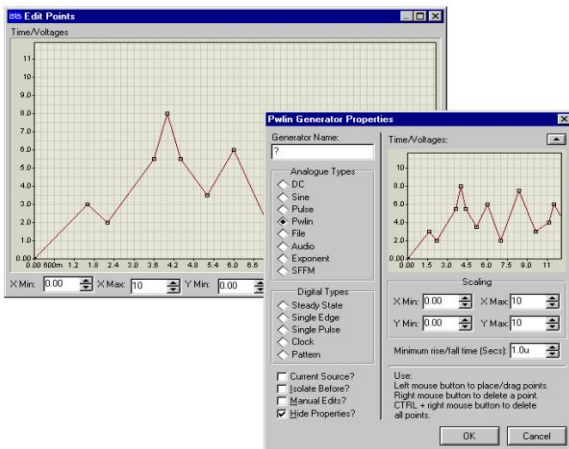
Excellent Modelling Tools

If you need to create your own component models, PROTEUS provides an excellent environment in which to do so. The support for hierarchical design in ISIS enables you to create a virtual test jig in which the component model can be developed. This means that any changes to the model can be evaluated quickly and easily prior to storing the model as a pre-compiled netlist.

Alternatively, you can use the VSM API to implement both analogue and digital models within Windows DLLs using a programming language such as C++. The VSM API can also be used to implement graphical functionality for complex animated components.

SPICE3F5 Simulator Kernel

PROSPICE is based around the industry standard SPICE analogue simulator developed at Berkeley University, California.



and contains the latest convergence techniques and primitive models. PROSPICE uses Berkeley's source code wherever possible, guaranteeing best possible compatibility both in terms of numerical results, and support for manufacturers' SPICE models.

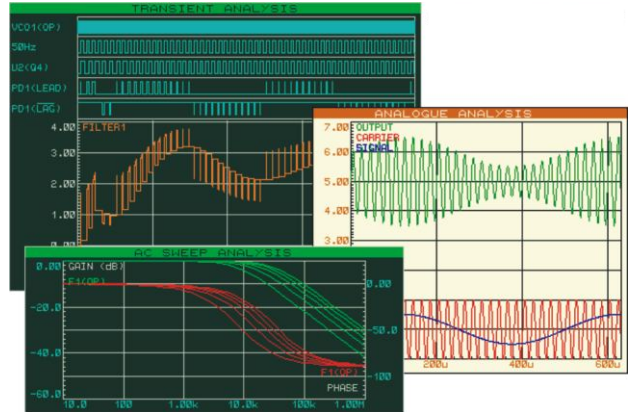
True Mixed Mode Simulation

PROSPICE incorporates a number of extensions to standard SPICE which allow it to model digital circuitry using an event driven paradigm. This is much more

efficient than attempting to model the transistor level behaviour. When both analogue and digital parts are present, both techniques are used in parallel giving optimum performance and accuracy.

Fully Compatible with Manufacturers' Models

More and more component manufacturers are providing SPICE models for their wares as well as the traditional data books. By choosing PROSPICE you will be able to gain



maximum benefit from this resource - we have made a point of using Berkeley code to parse the SPICE netlists in order to guarantee best possible compatibility. And to get you started, we have gathered over 5000 SPICE models from the Internet and linked them to appropriate schematic symbols in ISIS.

Feature Rich Digital Simulation

PROSPICE incorporates a fully featured event driven digital simulator which is automatically invoked whenever digital components are present. The digital simulation paradigm correctly models timing, glitch behaviour, floating inputs and undefined states - beware that not all so called mixed mode simulators are anything like as good.

PLD Modelling

PROSPICE includes special digital primitives which represent PLD fusemaps. These devices can be used to construct models of *any* programmable logic device. Specific models for popular PLD devices are included in the supplied component libraries.

The information on how the device is programmed is read directly from the JEDEC file produced by your PLD assembler. Therefore, you are not tied to using any particular PLD development system.

Conformance Analysis

This unique feature compares a new set of simulation results against reference data at pre-determined sampling points. Coupled with VSM co-simulations of embedded software, it becomes an extremely powerful quality assurance tool; changes to the hardware or software can be checked for unwanted side effects entirely automatically.

"Once again, Labcenter has concentrated on the essentials and presented these in depth rather than provide a lot of peripheral features of marginal use. In doing so it has produced an excellent all round simulator. You are unlikely to be in a position of requiring a particular basic simulation in detail, but finding that the program does not provide it, as you may be with other programs in this sector of the market."

Electronics & Wireless World Review

ARES Advanced Routing & Editing Software

Our high performance netlist based PCB design software perfectly complements ISIS. Incorporating both automatic component placement and a highly effective rip-up and retry auto-router, ARES transfers both time and effort from you to your PC. On the other hand, if you prefer to route your boards manually, the system places relatively few restrictions on how you go about the task.

PCB Design

Features

- Layers: 16 copper, 2 silk screen, 4 mechanical plus board edge, keepout, resist and solder mask.
- Any angle component placement and pad-stacks.
- Fully automatic ratsnest and force vector generation.
- Drag and Drop pin-swap/gateswap.
- Acclaimed manual routing system is ideal for netlist based manual routing.
- Gridless, polygonal power planes with full control of fill style and thermals.
- Connectivity and physical design rule checkers to prove design integrity.
- Package library includes over 1000 standard footprints.
- Output to any Windows device including pen plotters.
- Full set of CAD/CAM output and panelization facilities.
- Pick and Place file for automatic insertion machines.

Design Automation

- Automatic Component Placement.
- Multi-strategy grid based auto-routing.
- Special routines for SMT fanouts.
- Rip-Up & Retry for 100% routing on most boards.
- Tidy pass reduces via count and track length.

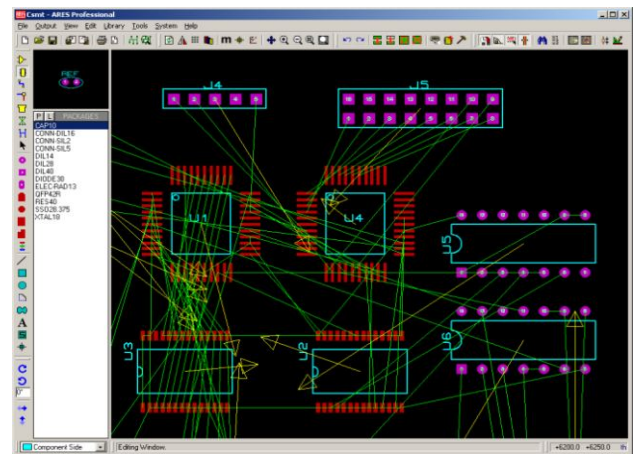
Layout Database

ARES features a state of the art layout database capable of representing the most complex of PCB designs. Placement resolution is 10 nanometers within a maximum board size of 20m. Components and other objects may be rotated in 0.1 degree increments whilst padstacks facilitate the achievement of maximum routing area on inner layers.

Netlist & Ratsnest Handling

During the placement phase, ARES displays both the ratsnest and force vectors. Both are updated in real time when you drag components. The ratsnest is also automatically updated during routing - add a track and a ratsnest line will disappear; delete a track and one will re-appear.

The system fully supports design modifications - if you change the schematic and re-load the netlist, ARES will flag up exactly which components and/or tracks are affected. Equally, pin-swaps and gate-swaps made in ARES are automatically fed back to the schematic.



Route Placement & Editing

Manual routing makes no requirement that you start from the ratsnest lines (rubberbanding). You can place tracking in any way you wish and ARES will remove ratsnest lines as the connections are actually completed.

When editing routes, you can re-route or delete any section of a track, irrespective of how it was originally placed. Commands are also provided to change the thickness and/or layer of any section of tracking.

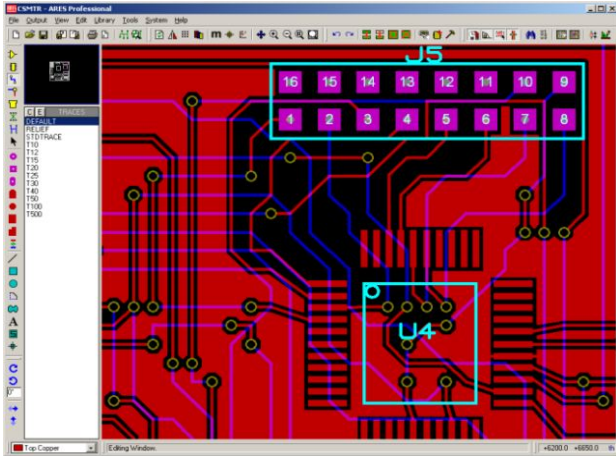
If thick tracks are laid between obstacles such as IC pads, ARES will automatically insert a narrower 'neck' in order to maintain the current design rules.

Curved tracks can be laid down simply by pressing the CTRL key and marking the route with the mouse.

Power Planes

ARES features the ultimate in power plane support - user placeable polygonal regions within which inner boundaries are automatically created around existing pads and tracking. Change the pads and tracking and the boundaries are recomputed to maintain design rule clearances.

Thermal reliefs are supported and you can choose whether to hatch or fill each polygon. All computation is based on gridless shape geometry and occurs *in the background* so that you can carry on working on the design.



Design Rule Checks

During manual routing, ARES checks each track as you place it and warns you if any design rules (physical/electrical) are broken. You can also run global physical and electrical design rule checks at any time. Double click any design rule error and ARES will show you its location on the board.

Package Libraries

The supplied libraries cover a large range of through hole components including all the most common IC, transistor, diode and connector packaging types. We also supply *as standard*, the full SM782 library for SMT footprints which includes all the standard discrete and IC packaging styles.

New packages can be created directly on the drawing whilst ARES also supports general 2D drafting features.

CADCAM Outputs

As well as providing the basic ability to output your PCB to standard Windows printers, ARES provides an optimized HPGL driver for pen plotters, and a full set of features for professional board manufacturing.

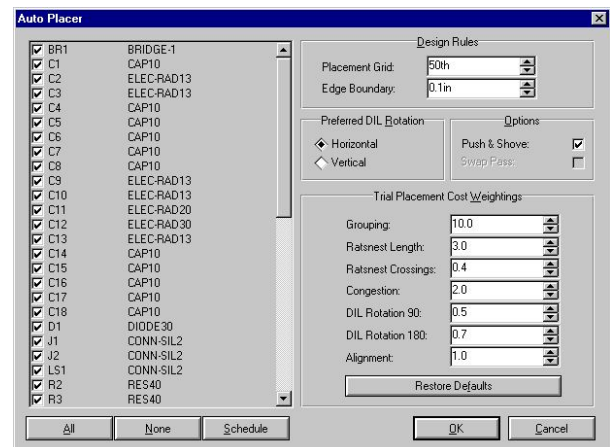
Gerber is supported in both RS274D and the newer RS274X formats whilst a standard Excellon format file is produced for drilling machines. In addition, an ASCII file

listing component positions and orientations is produced for use with Pick and Place machinery.

A Gerber Viewer is also provided allowing you to check that Gerber files contain the expected data, and to panelize boards prior to issuing them for manufacture.

Auto-Placement

Automatic component placement makes it possible to design an entire board with the absolute minimum of effort on your part. Alternatively, since the placer can operate interactively, you can pre-place critical components first and let ARES auto-place the rest.



Auto-Routing

Our grid based router is both flexible and fast and can route using any track thickness or via width, at 90 or 45 degrees, and on 1-8 layers. It was placed in the top Category A in Electronics World's most recent review of PCB software.

The range of routing grids available enables you to trade off routing density against execution speed with densities of 1, 2 or 3 traces between IC pads. The router also has special routines which enable it to form 'fan outs' from rows of SMT pads which would otherwise be off grid, thus enabling it to perform well with boards containing SMT parts.

The Rip-Up & Retry mode enables it to remove and replace tracks which block others giving 100% completion on most medium density boards routed at 50 or 25 thou. Meanwhile, our innovative costing/scheduling logic reduces the via count by as much as four fold over other low-medium cost routers.

Finally, you can run a tidy pass which reduces both track length and via count whilst improving the aesthetic quality of your board at the same time.

"PROTEUS from Labcenter stands out as the best all-round program in this review. While the other programs reviewed have strengths at various places in the pcb design process, Proteus maintains a constant high level of capability throughout. Whether it is a well turned out schematic, user-friendly interactive routing, effective and configurable auto-placing, competent autorouting, or a combination of autorouting and interactive routing, PROTEUS handles everything very well."



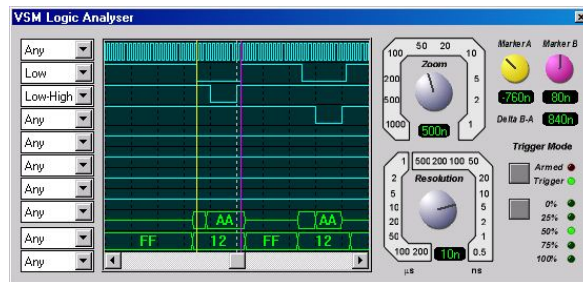
Virtual System Modelling

Proteus VSM is an extension of the PROSPICE simulator that facilitates co-simulation of microprocessor based designs including all the associated electronics. Furthermore, you can interact with the microcontroller software through the use of animated keypads, switches, buttons, LEDs, lamps and even LCD displays. Please refer to the separate leaflet for further information.

Features

- CPU models available for many popular micro-controllers including PIC, AVR, HC11 and 8051.
- Interactive device models include LED and LCD displays, RS232 terminal, universal keypad plus a range of switches, buttons, pots, LEDs, 7 seg displays and more.
- Extensive debugging facilities including register and memory contents, breakpoints and single step modes.
- Source level debugging for selected development tools including IAR C-SPY and Keil uVision 2.

- Integrated 'make' utility - compile and simulate with one keystroke.
- DLL interfaces for application specific models. Full documentation supplied with the package.



THE PROTEUS PCB DESIGN PRODUCT RANGE

Proteus PCB Design is available in five levels offering a range of design capacities and features to match your application. Level 1 is limited on both pin count and features whilst Level 2 is limited only in terms of design capacity and offers the full set of features. Level 3 is completely unlimited.

The PROSPICE mixed mode simulator is also available as an option for any of the levels, should you not require the microprocessor simulation capability offered by Proteus VSM Professional.

PROTEUS PCB DESIGN	LEVEL 1/1+	LEVEL 2/2+	LEVEL 3
Max Number of Pins in Netlist	1000/2000	1000/2000	Unlimited
Shape based power planes	1 per layer	Unlimited	Unlimited
Standard Auto-routing	✓	✓	✓
Rip-up and Retry Routing		✓	✓
Auto-Placement		✓	✓
Gate-Swap Optimizer		✓	✓

PCB DESIGN LIMITS

PROTEUS Levels 1 and 2 impose a limit for the number of pins in the netlist. These limits apply when loading it into ARES. Any number of pins may be placed on the PCB itself, however, enabling you to exceed the limit by the odd component should the need arise.

Levels 1+ and 2+ offer double the design capacity but are otherwise identical.

POWER PLANES

All levels of PROTEUS handle power planes using shape

based polygon merging. However, in Level 1, only one power plane is allowed per layer - partial power planes and multiple power planes on one layer are supported in Levels 2 and 3 only.

AUTOROUTING

All PROTEUS Levels include a sophisticated multi-strategy autorouter.

In Levels 2 and 3, you also get rip-up and retry operation which will give 100% completion on all but the most complex or densely packed boards.



UK Product - PROTEUS is developed entirely by ourselves so we are able to give unrivalled backup and technical support.

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